RESEARCHERID
THOMSON REUTERS

[Saxena * *et al.*, 6(9): September, 2017]
IC™ Value: 3.00

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

IJESRT
INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

A SCALLING CRITERIA OF FUNDAMENTAL SOI DESIGN DEVICES

Ritu Saxena[*1] & Ass.Prof. Shiva Bhatnagar[2]
[*1]M. Tech Student (VLSI Design), Patel college Indore(M.P.).
[2]Asst. Professor, Dept. of ECE, Patel college Indore(M.P.).

DOI: 10.5281/zenodo.995979

ABSTRACT

The driving force for the semiconductor industry growth has been the elegant scaling nature of CMOS technology. In future CMOS technology generations, supply and threshold voltages will have to continually scale to sustain performance increase, limit energy consumption, control power dissipation, and maintain reliability. These continual scaling requirements on supply and threshold voltages pose several technology and circuit design challenges. One such challenge is the expected increase in threshold voltage variation due to worsening short channel effect. This thesis will address three specific circuit design challenges arising from increased threshold voltage variation and present prospective solutions. First, with supply voltage scaling, control of die-to-die threshold voltage variation becomes critical for maintaining high yield. An analytical model will be developed for existing circuit technique that adaptively biases the body terminal of MOSFET devices to control this threshold voltage variation. Based on this model, recommendations on how to effectively use the technique in future technologies will be presented. Second, with threshold voltage scaling, sub-threshold leakage power is expected to be a significant portion of total power in future CMOS systems. Therefore, it becomes imperative to accurately predict and minimize leakage power of such systems, especially with increasing within-die threshold voltage variation

I. INTRODUCTION

Designing Integrated Circuits for portable electronic devices are essential is challenging as they are energy constraint. The ICs for such devices should be made energy efficient in order to let the devices operate long time. As many wireless, small handheld devices with innovative technologies came into existence, they are capable of processing multimedia or digital signal processing applications. As a matter of fact, the multimedia applications such is very complex in terms of mathematical complexity [2] causing more power consumption in hand held multimedia enabled devices. This warrants new VLSI technique implementations for making such devices energy efficient. Many techniques came into existence for reducing power consumption in VLSI designs. They include dynamic voltage frequency scaling, multiple supply voltages, threshold-voltage controlling, power-down techniques, clock gating, switched-capacitance reduction, and voltage scaling [3], [6]. All these techniques are efficient in reducing power consumption with some cost due to multimedia designs. They achieve it by reducing dynamic power that has significant share in power dissipation. To improve the power saving features in VLSI designs, this paper proposes a novel technique that ensures low power dissipation while supporting two kinds of designs that have various capabilities. The existing techniques explored in [7]-[1] that focus on reducing dynamic power minimizing switched capacitance. In case of [7] while making arithmetic operations, the un used parts are turned off in order to reduce power consumption. This technique is known as partially guarded computation. It could reduce power usage up to 44% with area overheads up to 36%. The drawback with this technique is that it can’t reduce power consumption in case of adders due to the kind of circuitry. A new adder was introduced in [8] which is a 32 bit model with two inputs namely sign extension and dynamic range determination in order to reduce power consumption. A multiplier is presented in [9] for effective dynamic range which resulted in Booth codes. Delay and area overheads are the two drawbacks of [9]. Glitching power minimization is the technique used in [1] for replacing existing gates with new ones which are equal in terms of functionality. It is capable of saving only 6.3% power dissipations. A double switched circuit block is used in [1] could reduce power dissipation during downtime.

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

II. LEAKAGE CURRENT

It has been established that to limit the energy and power increase in future CMOS technology generations, the supply voltage (V_{dd}) will have to continually scale. The amount of energy reduction depends on the magnitude of V_{dd} scaling. Along with V_{dd} scaling, the threshold voltage (V_t) of MOS devices will have to scale to sustain the traditional 30% gate delay reduction. These V_{dd} and V_t scaling requirements pose several technology and circuit design challenges. One such challenge is the rapid increase in sub-threshold leakage power due to V_t scaling. Should the present scaling trend continue it is expected that the sub-threshold leakage power will become as much as 50% of the total power in the 0.09 m generation as shown in Figure 2-5. Under this scenario, it is important to be able to predict sub-threshold leakage power more accurately. Present leakage current estimation techniques do not take into account the variation in within-die threshold voltage. It will be shown that this assumption leads to significant inaccuracies. A mathematical model for chip leakage current that considers within-die threshold voltage variation will be derived. Microprocessor measurements that verify the improvement in leakage estimation with the new model are also presented. In rest of the chapter, the term leakage refers to sub-threshold leakage.

III. SEMICONDUCTOR DEVICE MODELING

The physics and modeling of devices in integrated circuits is dominated by MOS and bipolar transistor modeling. However, other devices are important, such as memory devices that have rather different modeling requirements. There are of course also issues of reliability engineering—for example, electro-static discharge (ESD) protection circuits and devices—where substrate and parasitic devices are of pivotal importance. These effects and modeling are not considered by most device modeling programs; the interested reader is referred to several excellent monographs in the area of ESD and I/O modeling. A model that predicts system leakage based on first principles will be presented and a circuit technique to reduce system leakage without reducing system performance will be discussed. Finally, due to different processing steps and short channel effects, threshold voltage of devices of same or different polarities in the same neighborhood may not be matched. This will introduce mismatch in the device drive currents that will not be acceptable in some high performance circuits. In the last part of the thesis, voltage and current biasing schemes that minimize the impact of neighborhood threshold voltage mismatch will be introduced.

IV. REVERSE LEAKAGE CURRENT

Reverse leakage current in a semiconductor device is the current from that semiconductor device when the device is reversing biased. When a semiconductor device is reverse biased it should not conduct any current at all, however, due to increased barrier potential, the free electrons on p side are dragged towards positive terminal of the battery, while holes on n side are dragged towards negative terminal of the battery. This produces a current of minority charge carriers and hence its magnitude is extremely small. For constant temperature reverse current is almost constant though applied reverse voltage is increased up to certain limit. Hence it is also called as reverse saturation current. The term is particularly applicable to is mostly semiconductor junctions, especially diode and thyristor.

Reverse leakage current is also known as "zero gate voltage drain current" with MOSFETs. The leakage current increased with temperature. As an example the Fairchild Semiconductor FDV303N has a reverse leakage of up to 1 micro amp at room temperature rising to 10 micro amp with a junction temperature of 50 degree Celsius. For all basic purposes, leakage current is very small, and, thus, is normally negligible.

V. PROPOSED SOI MOSFET DESIGN

- **Silicon on insulator** (**SOI**) technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance. SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or sapphire (these types of devices are called silicon on sapphire, or SOS). The choice of insulator depends largely on intended application, with sapphire being used for high-performance radio frequency (RF) and radiation-sensitive applications, and silicon dioxide for diminished short channel effects in microelectronics devices. The insulating layer and topmost silicon layer also vary widely with application
- **Need to SOI design** The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic devices, colloquially referred to as

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

"extending Moore's Law" (or "More Moore", abbreviated "MM"). Reported benefits of SOI technology relative to conventional silicon (bulk CMOS) processing includes:

- Lower parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance.
- Resistance to latch up due to complete isolation of the n- and p-well structures.
- Higher performance at equivalent VDD. Can work at low VDD's.
- Reduced temperature dependency due to no doping.
- Better yield due to high density, better wafer utilization.
- Reduced antenna issues
- No body or well taps are needed.
- Lower leakage currents due to isolation thus higher power efficiency.
- Inherently radiation hardened (resistant to soft errors), thus reducing the need for redundancy.

VI. RESULTS AND SIMULATION

1. Level 1 analysis

(W=3, L=1Micrometer)

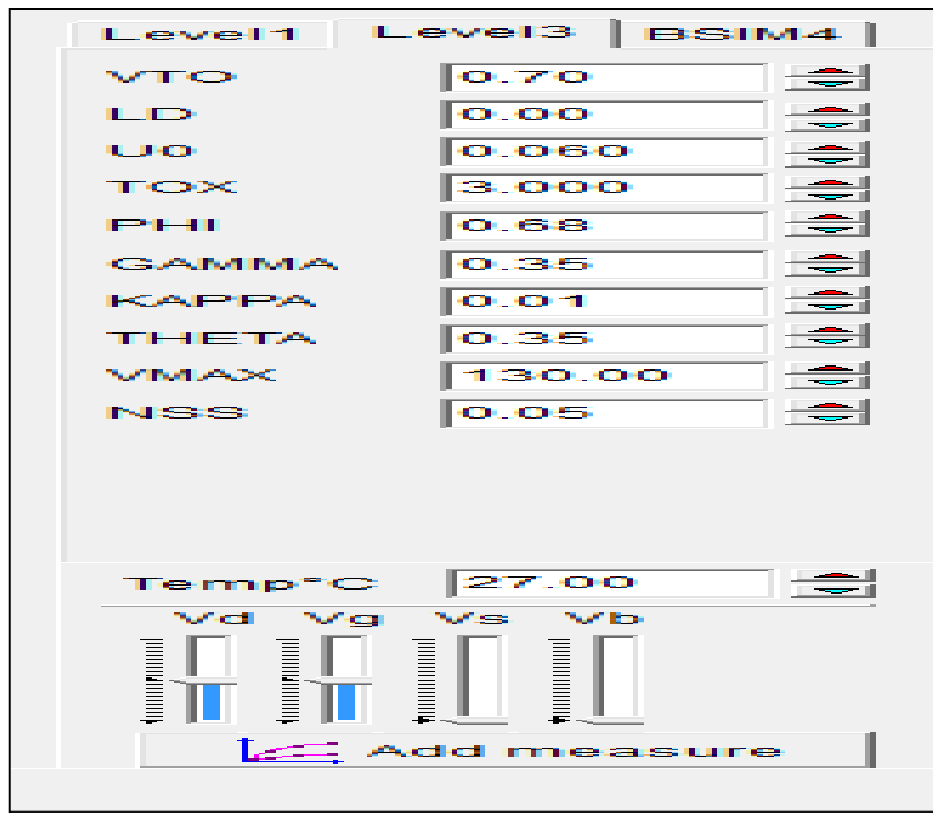
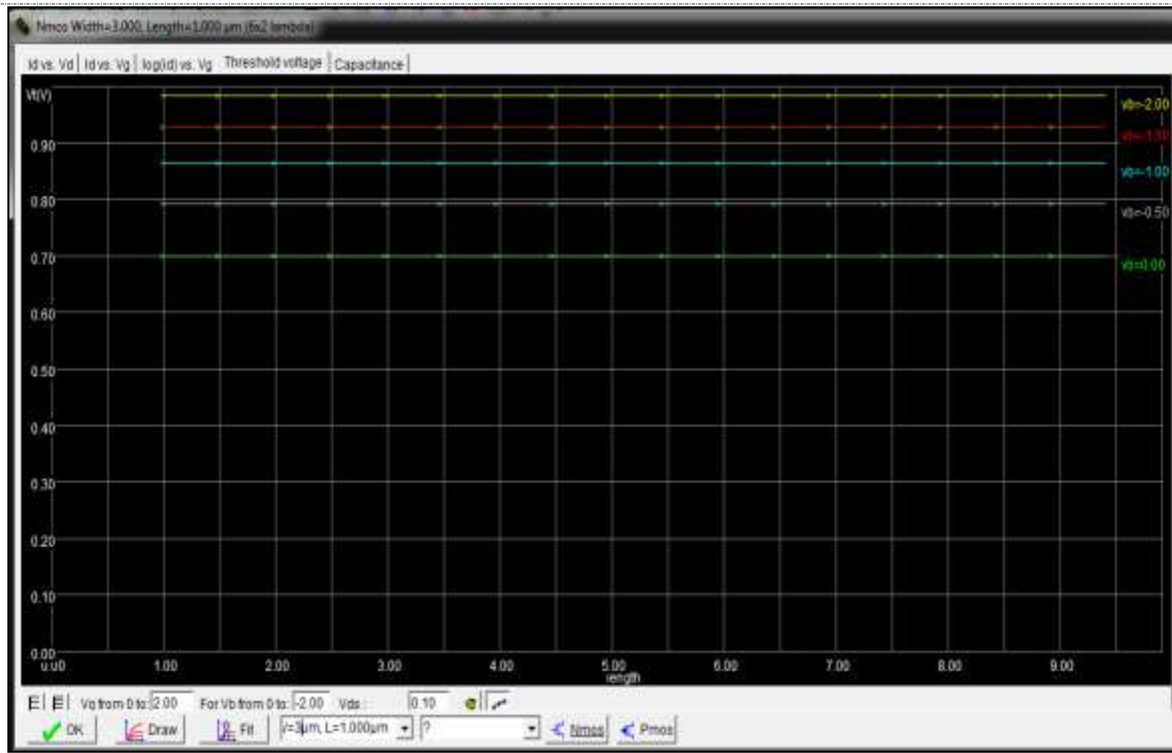


Fig (6.1) level 1 analysis

Threshod Voltage= 0.70
Effective Lengh=0.00
Thickness=3.00
Work Fuction=0.68

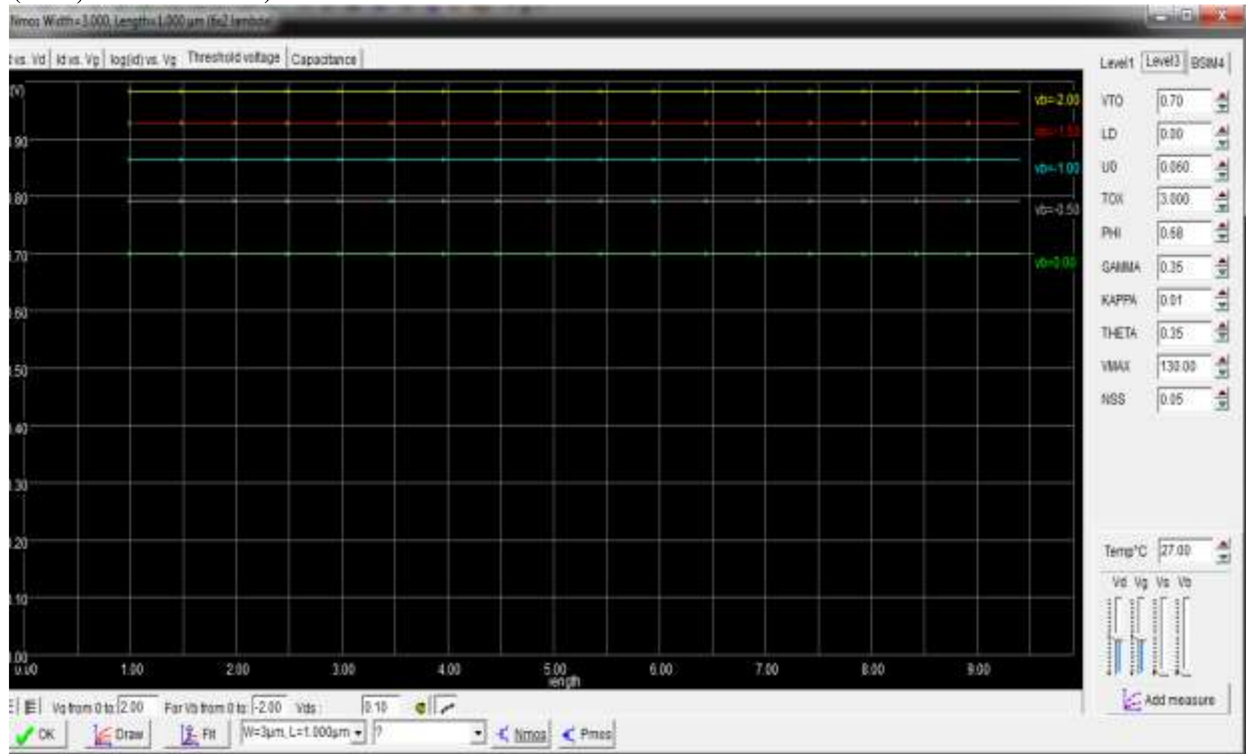
ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7



Different colored line shows voltage and blue line show average voltage.

2. **Level 3 analyses**

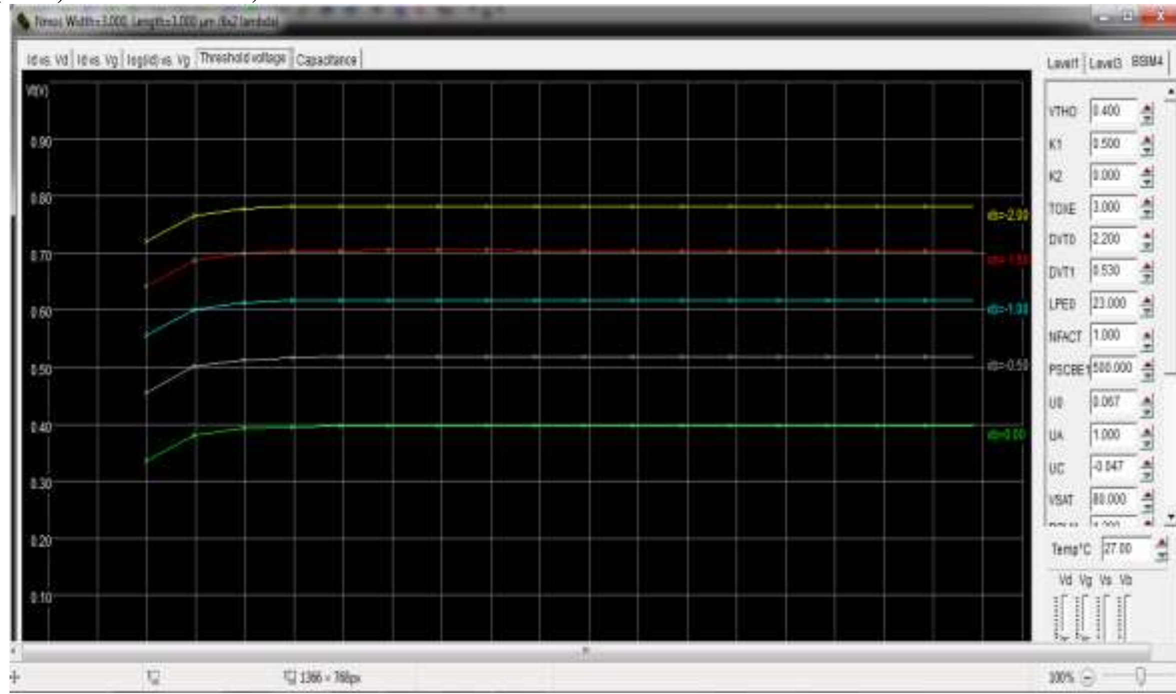
(W=3,L=1Micrometer)



ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

3. BSIM (berkeley short-channel igfet model):

(W=3, L=1Micrometer)



PREVIOUS SCALLING TABEL

Lg (um)	Ob, Od for Vt-target	Ob, Od for Vt-nom	Ob, Od for Vtnom with (bias)	Ob, Od for Vt-low	Ob, Od for Vtlow with (bias)
0.25	0.78, 15	0.76, 17	0.74, 18 (0.24)	0.74, 20	0.68, 25 (0.66)
0.18	0.74, 21	0.72, 24	0.69, 27 (0.31)	0.70, 29	0.59, 40 (1.13)
0.13	0.70, 32	0.68, 38	0.62, 44 (0.49)	*0.65, 44*	*0.52, 64 (1.34)*

PROPOSED SCALLING RESULT

Lg (um)	Ob, Od for Vt-target	Ob, Od for Vt-nom	Ob, Od for Vtnom with (bias)	Ob, Od for Vt-low	Ob, Od for Vtlow with (bias)
0.25	0.78, 15	0.76, 17	0.74, 18 (0.24)	0.74, 20	0.68, 25 (0.66)
0.18	0.75, 19	0.73, 23	0.71, 25 (0.28)	0.71, 27	0.63, 34 (0.84)
0.13	0.73, 28	0.71, 33	0.67, 36 (0.34)	0.68, 39	0.57, 53 (1.26)

RESEARCHERID
THOMSON REUTERS
[Saxena * *et al.*, 6(9): September, 2017]
IC™ Value: 3.00
ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

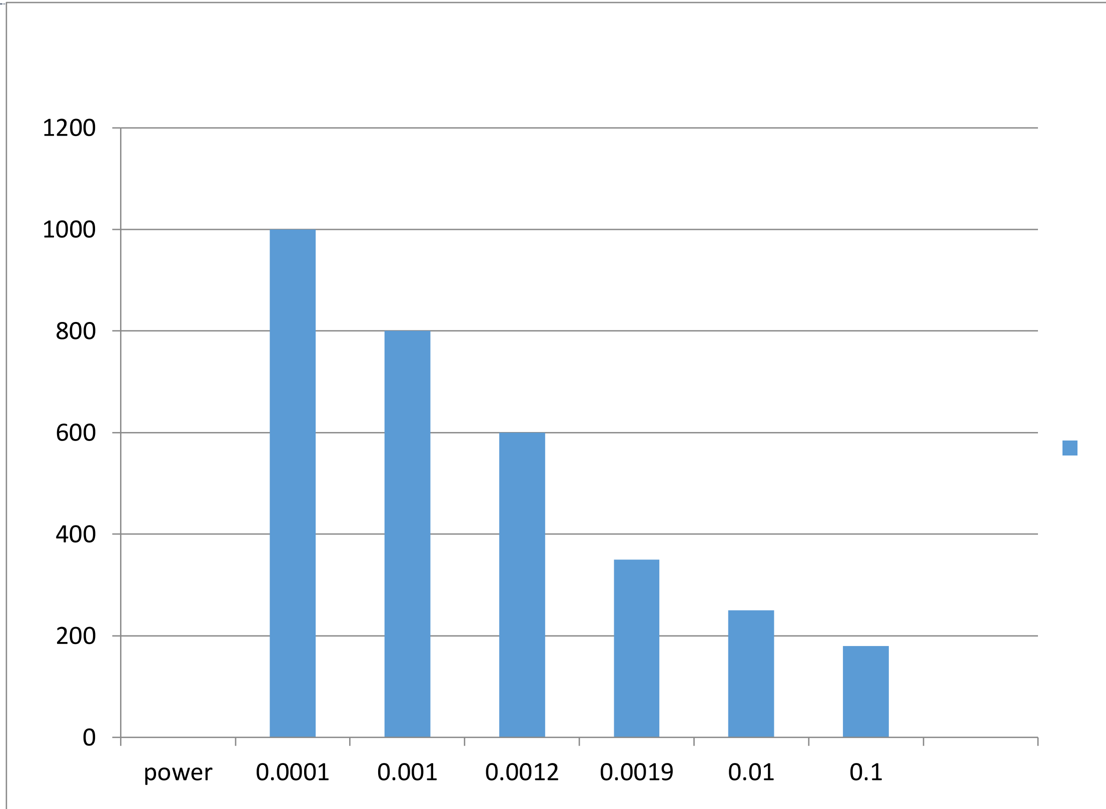


Fig (6.2) Power and nano scale sizing effect in MOSFET.

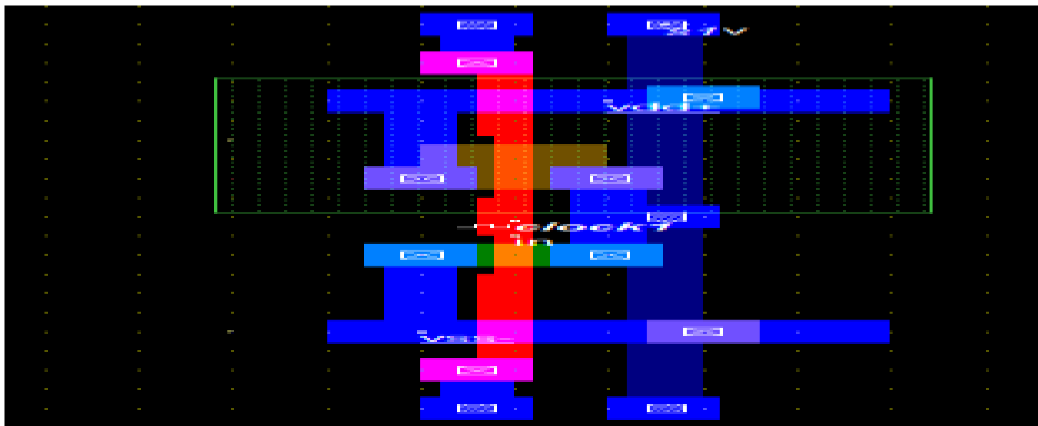
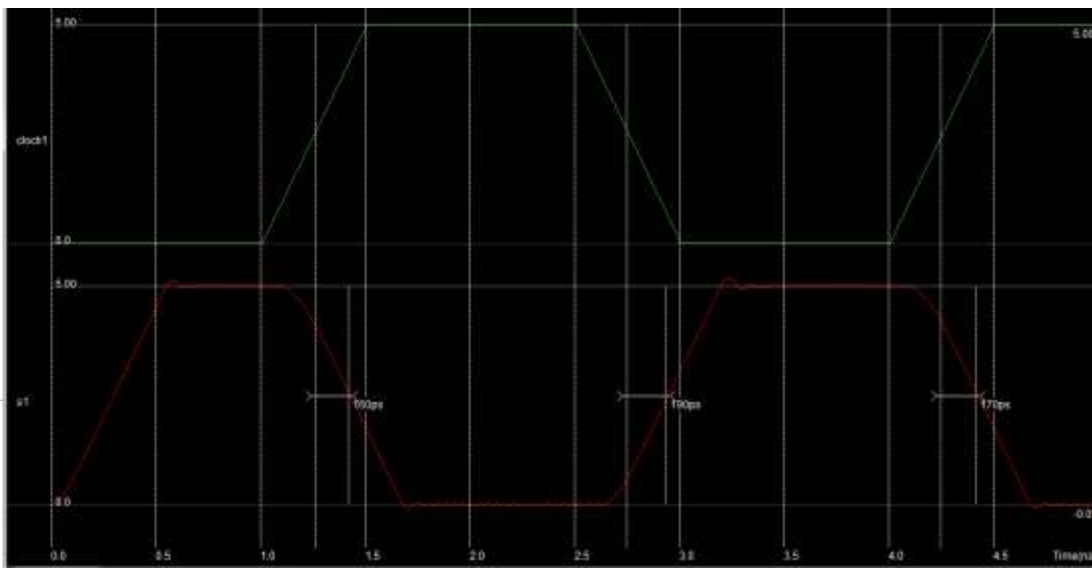


Fig (6.3) Not gate Layout.



ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

Fig (6.4) Timing waveform.

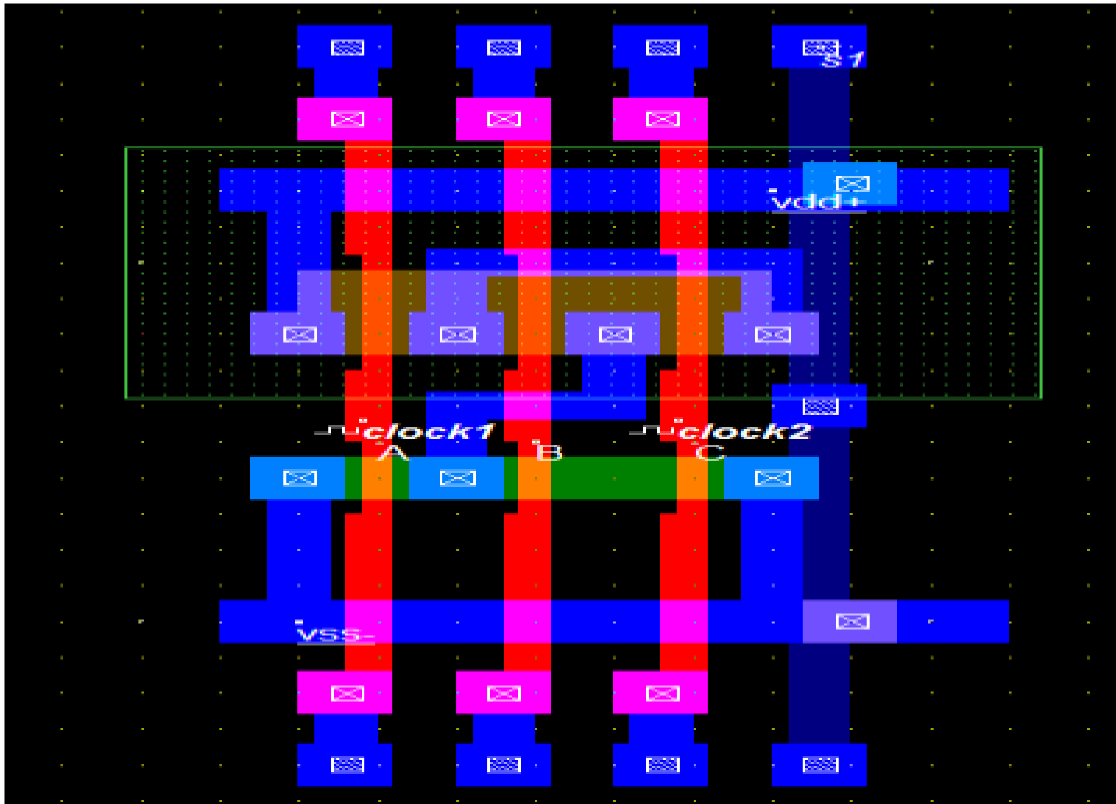
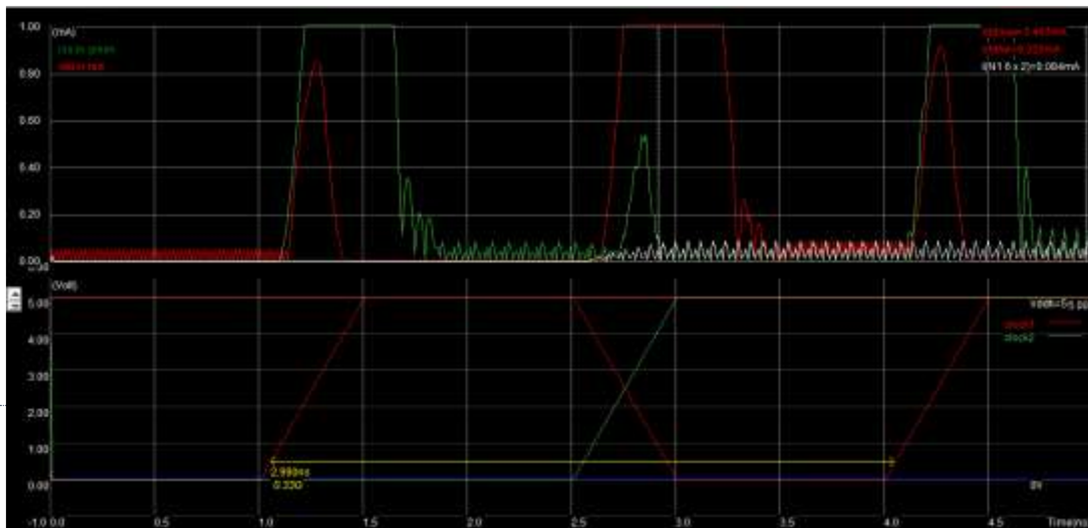


Fig (6.5)Nand gate Slice



ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

Fig (6.6) Delay waveform.

Comparison table Old Vth and Proposed Vth.

DESIGN	Vth(old)(v)	(Proposed tech.)Vth(v)
NAND	2	1.7
NOR	2.2	2.0
RAM	3.8	3.4
ROM	4	3.67
SLICE	3.2	3.2
FLIP FLOP	3.6	3.2

The first graph presents the change switching time with respect to variation in aspect ratio. It is important to see these results because it's the main thing which will affect the speed of the device.

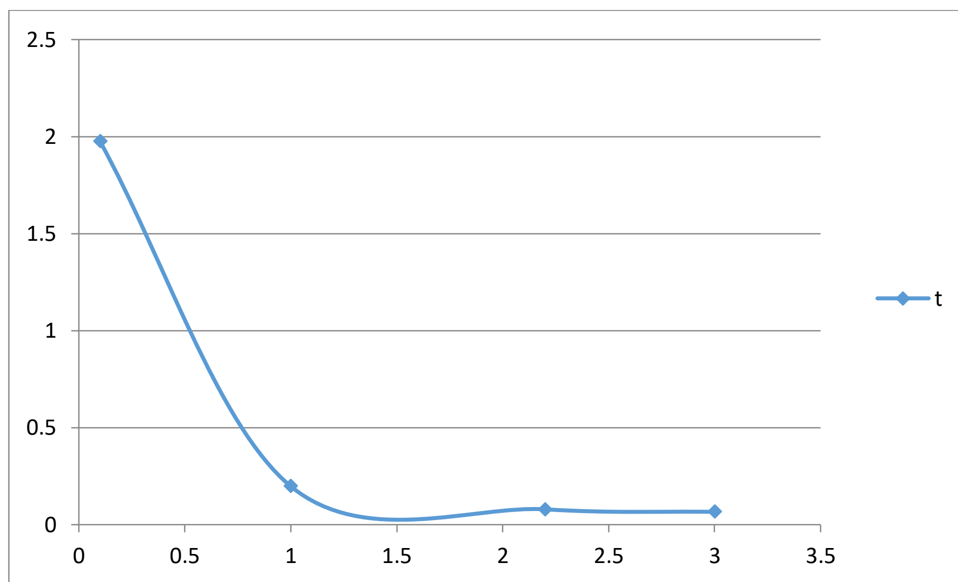


Fig (6.7) Graph between switching time & aspect ratio

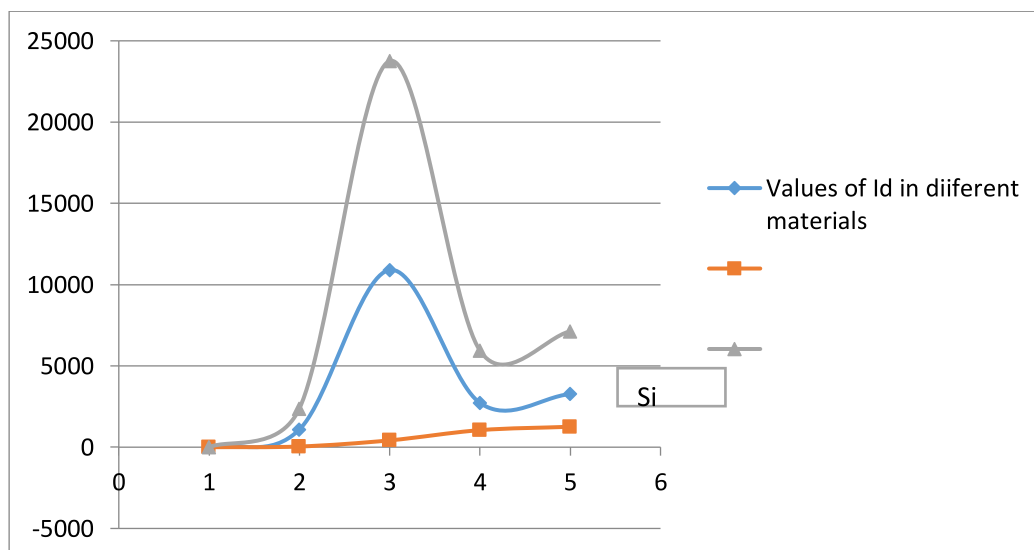


Fig (6.8) Graph represents Drain current of Ge

ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

VII. CONCLUSION

One important aspect that was not covered in this thesis is the increasing importance of supply voltage variation. The variation in supply voltage is due to iR and L di/dt drops in the power grid with non-zero parasitic resistance (R) and non-zero loop inductance (L). Ideally, one would like to maintain the historical 10% variation is supply voltage. This is becoming harder due to increase in the current level and the rate of change of current due to faster switching as technology is scaled. In addition, the parasitic resistance and inductance have not been reducing at the same rate as Increase properties of current flow. This problem is compounded by the fact that the supply voltage is expected to scale with technology. Traditionally, passive on-die and off-die decoupling capacitors were used to filter power supply noise. Delivering 500 W at 250 mV supply voltage is a very challenging problem due to high power supply current and low power supply voltage.

VIII. REFERENCES

[1] MAHENDER VESHALA, "CMOS Digital Integrated Circuit Analysis and Design", page-208, 3rd Edition, Tata McGraw Hill publication 2011.
[2] MAKARA TANG, "CMOS VLSI Design: A Circuit and System Perspective", 4th Edition,
[3] "RONALD D. SCHRIMPF," Modern VLSI Design, 3rd Edition (I.P. Based Design) 4th Edition prentice hall publication 2008
[4] JUN MA, "Application -Specific Integrated Circuits (ASICs)", IJETE, Volume 1 Issue 2, pp- 40-44, March 2014.
[5] SIVA G. NARENDRA, Divakar Shahi, Sh. Nishant Tripathi, "Design of 1.2Volt, 1GSPS, 2, 3, 4And 6 Bit Flash ADC Using EIS Comparator and Fat Tree Encoder", IJAERT, Volume 2 Issue 6, pp- 206-210, September 2014.
[6] G.SRINIVASULU, "Design of8 Bit ALU Using Microwind 3.1", IJAERT, Volume 2 Issue 2, pp- 50-55, May 2014.
[7] ELHAM KHAYAT MOGHADDAM, "Design of Charge Shared Power Optimized Pulse Triggered Flip Flop", IJETE, Volume 1 Issue 10, pp- 248-252, November 2014
[8] R. PRASHANTH, Devesh Kaushik, Preeti Sharma, Rahul Kumar, Puneet, Gyan Prakash Pal, "Congestion Control in an Internetwork", IJETE, Volume 1 Issue 9, pp- 217-220, October 2014
[9] SUMIT SINGH, Parikha Chawla, "Design & Analysis of High Speed Low and Area CMOS based Comparator with Different Architectures", IJETE, Volume 1 Issue 7, pp- 182-185, August 2014
[10] TRIPATI SUBUDHI, Rajesh Mehra, "Design Analysis of CMOS Voltage Mode SRAM Cell using Different nm Technologies", IJETE, Volume 1 Issue 3, pp- 76-80, April 2014.

CITE AN ARTICLE

Saxena, R., & Bhatnagar, S., Ass. Prof. (2017). A SCALLING CRITERIA OF FUNDAMENTAL SOI DESIGN DEVICES. *INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY, 6*(9), 520-529.